II. Brief Introduction of the Project

(*Involved field of science and technology, main technological contents, authorized patents, technical and economic indicators, and application and promotion*)

Analog Front-Ends (AFE) Interface Integrated Circuits (IC) plays an important role in most modern signal processing and wireless communication systems. Although extensive signal manipulation is performed by complicated digital signal processing (DSP) circuitry, the ultimate target of various electronic systems is to provide useful services to the human life. To move most complicated functions into digital domains actually will imply very high requirements on the Analog Front-End (AFE) Interfaces. To achieve satisfactory performance, the AFE should be implemented in advanced deep-submicron or nanometer CMOS to fully explore the advantages of emerging scaled-down technologies. Two main topics of Analog Front-End (AFE) Interfaces are investigated with nanometer CMOS technology: (i) **High-Speed, High-Resolution, Low-Power and Comprehensive Analog-to-Digital Conversion System**, (ii) **Wireless Circuits and Systems for Mobile TV Applications**.

(i) Analog-to-digital-Converter (ADC) plays an important role in most modern signal processing and wireless communication systems where extensive signal manipulation is performed by complicated digital signal processing (DSP) circuitry. As the continue advance of semiconductor fabrication technology and down scaling of silicon devices (e.g. nowadays CPUs are fabricated in very advanced 90nm and even 65nm CMOS technology), complex digital integrated circuits (ICs) can be achieved with high operating speed, small silicon area and low power consumption. As a results, manipulating signals in digital domain is highly desirable as the advantages of digital circuits can be fully benefited, e.g. digital circuits are less expensive to design and manufacture; flexible implementation through programming; and noise immunity of digital circuits provide superior dynamic range than their analog counterpart. Owing to the aforementioned advantages, more and more analog functions (including filtering, down conversion, modulation and demodulation) are performed in digital domain. With such a trend, the high operating speed of digital circuits can be fully utilized, emerging high-speed digital applications such as Medical Imaging, High-Definition Television (HDTV), Single-Chip CMOS Transceiver, Ultra-Wide-Band Transceivers, as well as flat-panel display (or LCD). Also, power/speed scalable options are also highly desirable for applications such as LCD, where different pixel resolutions require different speed requirements.

However, the ultimate target of various electronic systems is to provide services to the human life. What we see, listen, speak and sense are all analog signals. Demanding to move most complicated functions into digital domains actually necessitate very high requirements on the most front-end Analog-to-Digital Converters (ADC) with high-speed and high-resolution while simultaneously low power consumption. Also to fully utilize the advantages of digital circuits, the ADC must be integrated with the digital circuits in advanced deep-submicron CMOS processes for low cost System-on-Chip (SoC), placing increasing challenges due to short channel effects and low supply voltage.

(ii) Large number of independently developed mobile TV standards worldwide has led to the demand of multi-band silicon tuners for cost minimization of the embedded handheld devices that are intended for global market sale. Presently, the most dominant mobile TV standards are: terrestrial – digital multimedia broadcasting (T-DMB), integrated services digital broadcasting – terrestrial (ISDB-T), MediaFLOTM, digital video broadcasting – handheld (DVB-H) and digital multimedia broadcasting – terrestrial (DMB-T).

From the implementation viewpoint, the digital back-end can be efficiently shared since those standards favor similar kinds of modulation and data coding. For the radio frequency (RF) front-end, however, state-of-the-art solutions still require dedicated RF circuits optimized for each band. Yet, with the advance of fabrication technologies, multistandard-compliant nanoscale CMOS system-on-chip (SoC) solutions using wideband techniques to cover multiple applications would have the highest potential to yield the optimum cost.

On the other hand, the advance in lithography to nanoscale nodes requires the systems to operate underneath a low-voltage supply for the reliability issue, but with a slightly scaled threshold voltage for reducing the leakage power. This unparallel downsizing leads to significant reduction of voltage headroom that bottlenecks the RF and analog circuit design. Addressing voltage constraints of ultra-scaled processes at low cost becomes critical in implementation. In this content, state-of-the-art solutions have shifted to different routes. High-voltage (HV)-enabled circuit techniques using an elevated supply voltage appear as a novel way to neutralize the tradeoffs due to insufficient voltage headroom, while the speed and area benefits of ultra-scaled transistors can be fully acquired. This idea will be further investigated in this research, particularly, for the multi-phase clock generation circuits.

Owing to the immaturity of high-performance and multistandard-compliant joint RF design of mobile TV tuners in the literature and industry, this research addresses the RF and analog circuit design of mobile TV tuners. The ultra-wideband (UWB) coverage is from 170 to 1700 MHz such that only one reconfigurable RF front-end is necessary to support multiple standards. Unlike the conventional design of single-standard TV tuners, concurrent reception over UWB necessitates the RF circuits to feature high reconfigurability, and high linearity to prevent desensitization by the high-power blockers. This design challenges, in conjunction with the design goals of low noise figure, low power and high gain, constitute hard tradeoffs to obtain a sensible balance is between. Being realized in nanoscale CMOS processes (e.g., 90nm, 65nm and 45nm), the circuit techniques developed has significant impact to the state-of-the-art research and development in RF design.

The project has trained/under training over 3 Post-Doctorial Fellows, 17 Ph.Ds, 29 M.Sc and 33. B.Sc students, led to a total of 12 international journal publications (11 SCIE-indexed) and 51 international conference paper publications (all indexed by EI & IEEExplore, 23 in CPCI-S), 2 published books from the largest renowned international publisher – Springer. Three conference papers are published in the International Solid State Circuit Conference (ISSCC) which is known as the "Chip Olympics", in which one paper received the “Silk Road Award” in 2011. 2 Int. papers are published in the IEEE Journal of Solid-State Circuits (SCIE,

IF=3.12, also the most downloaded journal from IEEE). One of the conference paper in the Asian Solid-State Circuits Conference (A-SSCC), known as “Asia’s Chip Olympics”, won the student design contest, ranking No. 1. The research project also leads to the establishment of the State-Key Laboratory of Analog and Mixed-Signal VLSI in Macau, under the support of the FDCT.

(*Not exceed 1,200 words*)