

II. Brief Introduction of the Project

(Involved field of science and technology, main technological contents, authorized patents, technical and economic indicators, application and promotion, talent cultivation, and promotion of science and technology progress in Macao)

With video and imaging products becoming more intelligent and sophisticated, the demand for technology providing higher levels of image processing, performance, flexibility and functionality have sky rocketed. The worldwide acceleration in the transition from analog to digital television transmission, movement to 3D and connected TV has also boosted the video and imaging service. According to IC Insights, the CAGR of DTV, 3DTV and Connected TV are forecasted with 5%, 62% and 38% increase from 2012-2014, and Asia Pacific will have a significant increase and is the fastest growing region when compared with North America, Europe and Latin America.

Not only the new TV set but also other home-entertainment equipments need to be either High-Definition (HD)-capable, Standard-Definition (SD)-capable as well as PC-Graphic (analog RGB)-capable. Therefore, the Video Analog Front-End (AFE) with multi-format capability has been a surge in momentum for video SoCs. To continue our leading position in video AFE area, which has been one of the main product lines after the creation of Macau company, with also respect to the new emerging market and technologies, the applied R&D for an advanced and reusable up to Full-HD (1080p) and Multi-Format (CVBS - PAL/NTSC/SECAM; S-video or Y/C; TV YPbPr components- 480i/p, 574i/p, 720p, 1080i/p, PC-Graphic RGB component - VGA, XGA, SVGA, UXGA, WUXGA) video AFE IP in 65nm CMOS has been conducted under the joint support from FDCT and company.

Such applied R&D activities has overcome the worldwide-level design challenges in video AFE in such deep-micron CMOS technology, thus leading to the worldwide 1st Video AFE IP in 65nm in the market with the following multiple key innovations:

- 1) **Architecture-level Innovations**, e.g. multi-supply domain operation (interface at 3.3V and core ADC at 1.2V) for reception of wide range video input formats to achieve high-speed up to 165Ms/s – 205Ms/s at high power efficiency which solves large-scale DTV SoC thermal issue, dedicated Programmable Gain Amplifier (PGA) and cut-off frequency & order switchable anti-aliasing filter to support CVBS, and different component inputs (YPbPr for HDTV, RGB for PC-graphic) with different its electrical characteristics requirement at minimum area and power overhead, reusable plug-and-play 3 or 4-channel V-AFE configure to fit market needs at fastest time-to-market.
- 2) **Circuit-level Innovations**: e.g. wide operation frequency 10-bit ADC (10-165 or 205Ms/s) with auto power scaling for different video standards, low-distortion linearity boosted video analog input multiplexer; Multi-function clamping circuitry for DC restoration for multi-video signal format; high-input-impedance wideband input buffer with embedded programmable wideband tunable anti-aliasing filtering; area-and power-efficient low-noise 3rd-order video anti-aliasing filter with new

single-ended to differential-ended (SE-to-DE) conversion techniques (**US Patent filed**); Duty-cycle restorer for speed enhancement, Semi-auto and full-auto calibration for channel gain /offset calibration to achieve lowest cost effective white-balance tuning for end-customer; on-chip low-cost 75ohms video buffer and Y/C linear-phase mixer and so on.

The developed innovations from this applied R&D have been well deployed from 65nm to multiple process nodes, e.g. 55nm, 40nm and 0.13um/0.11um with all silicon-proven records (except 40nm under process of validation) for different market segments, thus proving its effectiveness, robustness and reusability. Therefore, the video AFE IPs have been well employed by consumer electronics chip player worldwide, e.g. 2 in Japan, 1 in Taiwan, 4 in mainland China, and 1 in the United States and others since 2008, including world/China leading Chip makers, e.g.¹. Toshiba, Nationalchip, SiS, IDT and so on. The direct total sales from all those video IPs over the past 4 years is about USD 4 Million (MOP 32 Million). Many of those customers have been in mass production with more than 5 million chip volume, which is corresponding to a conservative estimation of around >USD 50 million (MOP 400 Million).

Such applied R&D with the resulting 1st SIP prototype of Video AFE and the advanced technical innovations at both architecture system and circuit level in 65nm CMOS not only consolidates the company's leading position in this area the market but also boosts the Macau local applied research ability for higher competitiveness with excellent real economic impact. This proves effectively as an excellent model adequate at this stage in Macau for applied R&D, which is the key sector for fast developing high-technology industry to link between university academic research and industry product development. Because, the applied R&D are mostly directly funded and driven by government in the surrounding area, e.g. Hong Kong Applied Science and Technology Research Institute (ASTRI), Taiwan Industrial Technology Research Institute (ITRI), Singapore The Agency for Science, Technology and Research (A*STAR) and Korea Institute of Science and Technology (KIST).

Such applied R&D has strategic value and creates solid foundation for Macau company to further accelerate the aggressive IP roadmap and healthy local company development plan, which will open great opportunities for Macau's young generation in devoting their careers in the Hi-tech development, thus also stimulating the momentum of Macau higher-education with also high-level academic R&D. This will not only contribute ultimately to multi-diversification of Macau industry, and the resulting usage of the advanced IP technology developed by Macau team from both rich national and international customer bases from such cutting edge semiconductor industry definitely has also created highest promotion and in fact elevated worldwide Macau science and high-technology development.

(Not exceed 1,200 words)

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