2． 項目簡介

(*項目所屬科學技術領域、主要技術內容、授權專利情況、技術經濟指標及應用推廣情況*)

The robust development of high performance consumer electronic devices, such as Tablet, media players, flat-panel display, high-definition TV, set-top box, Ultra Wideband applications, 4G LTE smart phones with strong image and real-time processing power, continued to improve the quality of the human life. The main driving force of such rapid improvement is the strong digital signal processing power of the microprocessors as a result of continuing down-scaling of advanced CMOS technology. However, the outside world is analog in nature, to access such strong digital processing power, data conversion interface bridged between the analog and digital domain are mandatory in all electronic devices. As the boundary between analog and digital moves towards more outward nature analog world, the requirements of low power, high speed and digital noise insensitivity of such interface become much higher and crucial, and indeed the most challenging bottleneck of many systems, this necessitates high demands on research of high-performance data converters.

The “Twelfth Five-Year Plan” of country Ministry of Industry and IT (MIIT) has also laid out the focus on “The development of communications Chips, mixed-signal data conversion chips (Specified for Advanced ADC/DAC), etc.” Besides, “Embedded high-speed, high-resolution ADC/DAC IP cores” is also part of R&D topics of critical technology and equipment research under the 16 major projects of national S&T guided by Chinese State Council to accelerate the incubation and development of the country’s strategic emerging industries.

The goal of the project, in line with the main trend, is to setup a comprehensive research platform for the R&D in the state-of-the-art Data Conversion Techniques in nanometer CMOS technology. The research categories have in common low power focus even if they answer to different research and industrial interests. In this platform, 4 research directions are the defined as follow:

A. Energy Efficient and Dynamic Low-Power Analog-to-Digital Converter Design

There are increasing trends to use dynamic elements to replace the static elements, like opamps in pipelined ADC. However the nonlinearity and operation speed of such dynamic elements will impose performance limitations in the ADC, thus presenting a new challenging research direction of a new class of sampled-data system.

Architectural innovations is our group main objective and achievement by effectively combining the inherent advantages of different ADC architectures to achieve optimized power and energy at various resolution and speed, e.g. binary-search, flash, folding, pipelined, Successive Approximation Register (SAR) and Interleaving and so on. Even with some intrinsically not full dynamic, our group has proposed very power efficient Pipeline-SAR with “Opamp sharing” and “Partial interleaving” techniques, and also extremely low energy folding flash ADC with “Passive Folding” and “1T Embedded Thresholds” techniques to enable fully dynamic operation. Furthermore, our proposed speed enhanced techniques and circuits optimization in the SAR feedback loop, ADC has achieved very high speed with low power. Also the proposed “2b/Cycle” and “Compact DAC Structure” techniques make the SAR ADC reach a worlds’ new level of speed and energy efficiency.

B. Digitally Enhanced Analog-to-Digital Converter

Aggressive CMOS technology scaling permits larger-scale and faster digital implementation of complex

algorithms. Thus, digital calibration to analog non-idealities is a new trend. However, gain/offset/timing-skew mismatches, and dynamic errors usually require complex algorithm and lead to large power and digital substrate noise. Accordingly, our group has developed simplified “Offset Calibration”, “Inter-Stage Gain Calibration” and “Ratio-based Gain Error Calibration” techniques to solve the gain and offset error through various schemes. Furthermore, also the developed “RMS-based” and “Nonlinearity Calibration” techniques solve the time-skew and split DAC error in Pipeline and SAR ADC, respectively.

C. Wideband CMOS Continuous-Time Sigma-Delta Modulator

The power dissipation of ADCs used in wide-bandwidth wireless application has steadily been decreasing. However, further reduction is necessary for the stringent requirement in battery powered applications. In recent years, Continuous-Time Sigma Delta (CTSD) Modulators have been moving towards signal bandwidths that enable usage in such high-speed wireless systems. Traditionally SD Modulators has been achieved in Discrete Time (DT). It is possible to implement a CT modulator, which has many advantages. Accordingly, our group has developed “Excessive-loop Compensation” and “Non-linearity Compensation” techniques for enhancing the resolution in CTSD Modulators.

D. Analog-to-Digital Converters for Biomedical Applications

Bio-signals converted via sensors from human body to an electrical signals, by nature, are low frequency, variable amplitude and frequently complex waveforms but very noisy. Therefore it requires a high resolution ADC to preserve the integrity of the converted signals. Moreover, biomedical instruments require very low power due to the heat limitation of embedded in patient’s body. Our group has developed the “MSB-bit transfer” to achieve extremely low power at low speed design, and by effectively combing the high-precision SD and low-power SAR technologies plus the proposed “Passive Adder” technique, a new architecture of ADC have been emerged with great potential for higher resolution bio-medical applications.

Such platform with 4 research direction and 14 key innovation technologies have substantially contributed to the impact of the society and worldwide in the research field of data converter ICs. The research results leads to a significant breakthrough of the state-of-the-art data converter performance in terms of energy efficiency, resolution and bandwidth, placing the University of Macau (UM) as one of leadership positions worldwide in data converters research area with well recognized and appraised by world most renowned experts in field, e.g. Rehzad Razavi (UCLA, US), Bram Nauta (U Twente, Netherlands), Boris Murmann (Stanford, US), Akira Matsuzawa (Tokyo Inst. Of Tech), 严晓浪(浙大).

Such recognition is further proven from the no. of published world’s top-class IEEE Solid-State papers including JSSC, VLSI, CICC, ESSCIRC, A-SSCC (13 in 2 years) within 2012-2013 is ranked as 2nd internationally with only 1 paper less than the no. 1 from Oregon State University. Indeed, UM is the sole university from Mainland including Hong Kong in the top 25, and bid the total numbers published by the whole Korea, India, Singapore, Australia, China and Hong Kong.

3 International and 1 National key Awards is achieved, including, both the 1st time nominated from China including Hong Kong, Invited Tutorial Speaker in 2013 IEEE A-SSCC Chip Olympic and also IEEE SSCS

Distinguisher Lecturer in Data Converter; also 2012 IEEE Solid-State Circuits Best Chapter Award - Macau Chapter; nationally by Scientific Chinese of the Year 2012 (IT & Electronics category); locally by Winner of Research Achievement by Macau Business Award 2013.

The research have nurturing/under training over 1 Assistant Professor, 3 Post-Doctorial Fellows, 1 invited Visiting Fellow, 6 Research Fellows, 10 Ph.Ds, 19 M.Sc and 11. B.Sc students, led to a total of 5 international journals (all SCIE-indexed) and 17 international conference publications (all indexed by EI & IEEExplore, 6 in CPCI-S, 9 in world-class solid-state conferences), Four of the SCI-indexed journal in IEEE Journal of Solid-State Circuits (Impact Factor 3.06, the most downloaded journal from IEEE and most cited journal in US patent) are listed as top download papers in either the whole Journal set or even in the whole IEEExplore database, showing the impact to and recognition by the peers internationally.

The authorized 5 US patents, and 5 patents (2 US, 3 Taiwan) to be approved, are highly competitive solutions to address the real industrial problems with wide range of applications in communication and consumer electronics with large volume needs in market. The industrialization is under process with the on-going/potential cooperation with leading industry partners, e.g. Synopsys, ST Microelectronics and Huawei, which is expected for great economic value in future.