二． 項目簡介

（*項目所屬科學技術領域、主要技術內容、授權專利情況、技術經濟指標及應用推廣情況*）

Big Data aided by beyond exa-scale data exchange makes our daily lives subtlety convenient and is also the cornerstone of “smart city”. With mass data from a tremendous amount of devices, the energy cost for data exchange (e.g., for cooling) substantially exceeds the hardware cost. It is thereby crucial to improve energy efficiency to facilitate the zeta-scale data exchange needed in the near future. Moreover, the carbon footprint for such a scale data exchange received more attention in recent years. To cope with President Xi's highlighted "China headed towards carbon neutrality by 2060”, ultimately-energy-efficient chips become imperative to empowering both expandable and environmental-friendly data exchange technologies.

This project focuses on the key technologies for the ultimately efficient wireless/wireline chips that enable a carbon-neutral zeta-scale data exchange capability. The major technological breakthroughs of this project, developed by the team from the State-Key Laboratory of Analog and Mixed-Signal VLSI of the University of Macau, are summarized in the following four parts.

1) Data Acquisition and Conversion Interfaces: High-performance data conversion chips enable the zeta-scale worldwide Ethernet access ability both in the data center and user side. Energy-efficient technologies are developed for the data exchange to reduce the cooling energy consumption of the data centers and strengthen the battery life of the portable devices. These inventions cover a series of revolutionary data converter chips with high-speed and low-power features, which leads to a compact data transfer system with a large throughput capacity, offering an ultimate data communication experience.

2) Wireline Circuits: high-performance and high-energy-efficient wireline circuits are the bottlenecks to ultimately realize the efficient SerDes chips, delivering ultra-high-speed optical/electrical data streams in the zeta-scale datacenters. We proposed a series of innovative techniques, such as better power efficiency tens-of-Gb/s clock and data recovery (CDR) circuits; lower reference spur calibration-free phase-locked loop (PLL); and higher peak figure-of-merit harmonic-shaping voltage-controlled oscillator (VCO).

3) Frequency Synthesizer and Oscillator: Power- and area-efficient frequency synthesizers and oscillators provide low-jitter clocks and local oscillators (LOs) for ADCs and wireless transceivers demanded by power-efficient data exchanging and processing applications. These inventions focus on exploring novel techniques at both circuit and system levels to improve the noise performance of the frequency synthesizers and oscillators while reducing the power consumption and chip area.

4) Radio Frequency and Wireless Circuits: Low-cost frequency-tunable radio-frequency transceivers allow local coordination of hubs and gateways via the 5G New Radio/Bluetooth technologies, while enabling efficient maintenance and software update from another cloud server for network security and stability. This invention covers the design of high-performance and low-power transceiver chips to ensure power savings and cost reduction by eliminating a number of bulky external components.

The techniques developed from this project was academically transferred via 28 IEEE journals (including 11 in the prestigious IEEE JSSC), and 10 papers in the IEEE Solid-State Conferences (Including 3 papers in the ISSCC), maintaining our leading position in the top research groups from Columbia University, Apple Inc. and Tsinghua University during the same period. In addition, this project has fostered high-caliber Ph.D. and Master students who won key awards in IEEE top conferences, including IEEE RFIC 2021 [Best Student

Paper Award] and IEEE A-SSCC 2020 Student Design Contest [Distinguished Design Award]. Besides, we are collaborating with several top IC companies in China, including Huawei Hisilicon, to transfer the knowledge to the industry.

（*字數不超過 1200 字*）