## 2． 項目簡介

(*項目所屬科學技術領域、主要技術內容、授權專利情況、技術經濟指標、應用推廣、人才培養及對澳門科技進步的推動作用等*)

USB, short for Universal Serial Bus, is an industry standard developed in the mid-1990s that defines the cables. USB is essential to almost all electronic application such as mobile phone, smartphone, multifunction printer, computer, digital TVs, media player seven nowadays, many kinds of home intelligent appliances has USB for power plug and data transfer to upgrade our life. Since different applications have different multitude of requirements, determining the functions' lineup that optimally serves a particular target application and the market demands high-speed capabilities, while keeping silicon area and power consumption to an absolute minimum, is a challenge commonly faced by both System-on-Chip (SoC) integrators and IP providers. Integrating USB IP that has been silicon-proven and optimized for different feature helps reduce system power, area, and cost in today's SoCs.

As designs migrate below 20nm FinFET process such as 16nm/14nm or 10nm, the challenge of integrating USB functionality becomes more complicated, as digital circuits follow Moore's Law, higher wafer costs can be justified through improved performance and higher gate density. Analog circuits such as USB PHY make extensive use of I/O devices and do not scale with process node in the same way as digital circuits that use primarily core devices. However, wafer cost of FinFET is significantly higher than in 28nm or 40nm. USB PHY must evolve and develop new architectures to reduce the overall area, e.g. 0.38mm^2 USB PHY in a 28nm would need to decrease to 0.19mm^2 in 16 FinFET to keep the silicon cost the same.

The area reduction requirement is not the only big challenge for USB PHY in advanced nodes. Developing USB PHY to enable customer to select the optimal implementation for their application without sacrificing the features or capabilities required for USB compliance certification. Power down features minimize battery drain when the PHY is inactive, while retaining all PHY states to enable fast, accurate power-on capabilities. In addition, USB PHY must support the popular USB Battery Charging v1.2 specification and the USB On-The-Go (OTG) v2.0 protocol. Minimize the number of pins needed on the SoC periphery to further reduce SoC area and cost. For higher competitiveness, to minimize development cost and maximize the design technology coverage with silicon right performance for all different foundries at different process nodes are one of most challenging tasks for IP developers.

From this applied R&D project, the developed ~12 key advanced innovations with respect to the innovations at both architectural and circuit-level perspectives have been well deployed for the USB PHY IP Platforms in 28- nm and 14/16-nm FinFET processes where the new platform development has also enabled the 1st USB PHY IP in FinFET available in IP market, which bring great opportunity for future SoC solution in new consumer electronics application.

Being the world No.1 USB PHY provider according to Gartner and FemtoPHY product is about total world USB market share of 17.5%, such IP platform development enables directly around 55.9 Million USD PHY IP sales value (447 Million MOP) for > 49 applying units which are all world leading electronics companies from USA, Europe, Japan, mainland China and Taiwan. Most of their products are in mass production and employed in market well-known consumer electronic devices and also other brand-named Tablet, smart phone, computer and so on. The very conservative estimation of mass production chip volume is > 441Million and the corresponding market value > 2205Million USD ( >17.6 Billion MOP).

The production of the advanced IP technology developed by Macau team by rich national/international brand-named customer bases at a cutting edge semiconductor industry have created highest promotion and elevated world widely Macau high-technology development position.

*（字數不超過 1200 字）*